Magnetic memories: from magnetic storage to MRAM and magnetic logic

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Back to the basics

Electrons carry a charge ➔ electronics

transfer of information

... and a spin

quantum mechanics: ➔ projection of angular momentum \( \vec{s} \) : \( \pm \frac{1}{2} \hbar \)

➔ dipolar magnetic moment \( \vec{m}_s = -g \frac{\mu_B}{\hbar} \vec{s} \)
Back to the basics

Electrons carry a charge \( \rightarrow \) electronics

transfer of information

storage

... and a spin \( \rightarrow \) magnetism

magnetic moments

magnetic storage
Outlook

- the basics of magnetic recording
- the basics of spin electronics
- the magnetic tunnel junction
- the principle of the “magnetic random access memory” or MRAM
- “spin angular momentum transfer” and the “Spin-RAM”
- towards magnetic logic chips
- beyond MRAM and Spin-RAM in solid state magnetic mass storage
- beyond MRAM and Spin-RAM in “spin logic”

Basics: magnetic energies for storage

“localized” atomic magnetic moment picture + basic magnetic energies

**Exchange interaction**

tends to keep parallel the atomic moments

"magnetization" $M$ in ferromagnets

$\mu = M \, V$

**Magnetic anisotropy energy**

total energy changes with the orientation of $M$

magnetic storage of the information

$\Delta E = KV$ >> $k_B T$
Basics: exchange interaction and magnetization

Zeeman energy: interaction with a magnetic field

\[ E = -V \vec{H} \cdot \vec{M} \]

+ Magnetic anisotropy energy: preserves orientation of magnetization after writing
Magnetic recording

1898: V. Poulsen’s Drum Telegraphone

1933: Ring type head
E. Schuller

1928-35s: Magnetic tape:
F. Pfeumer / BASF-AEG

1953: Magnetic core memory

1956: First HDD - IBM RAMAC

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**Speed:** the natural dynamics of the magnetization

The Landau-Lifshitz-Gilbert (LLG) equation

\[
\frac{d\mathbf{M}}{dt} = -\gamma \mu_0 (\mathbf{M} \times \mathbf{H}_{\text{eff}}) + \frac{\alpha}{\mu_0} \left( \mathbf{M} \times \frac{d\mathbf{M}}{dt} \right)
\]

damping torque

*Damped precession* of the magnetization \( \mathbf{M} \) around its equilibrium axis

*Effective field* \( H_{\text{eff}} \): all the magnetic energies

*Precession frequency*: \( f = f_0 H_{\text{eff}} \)

\( f_0 = 28 \text{ MHz} / \text{mT} \quad (= 2.8 \text{ GHz} / \text{kOe}) \)
Precessional dynamics
in thermally activated reversal

Néel - Brown reversal =
thermally activated precessional behavior within the energy well
⇒ attempt frequency function of \( \alpha, K_U, \ldots \)

Non volatility: thermally excited switching

The "magnetic non volatility"

Long term stability of the magnetic storage:
spontaneous reversal of the magnetization due to thermal activation

\[ \Delta E = KV \]

Néel – Brown model
probability \( P \) for no reversal
after a time \( t: \quad P = e^{-t/\tau} \)

\[ \tau_0 \sim 1 \text{ ns} \]

\( k_B T \) = thermal energy
\( T \) = temperature

\( \tau = \tau_0 \exp(\Delta E / k_B T) \)

\( \text{ex: stability on } 10 \text{ years } = 3 \times 10^8 \text{ s} \)

"soft" error

\( I-P = 10^{-6} \quad KV \sim 54 \ k_B T \)

\( I-P = 10^{-12} \quad KV \sim 68 \ k_B T \)
The necessary compromise in magnetic recording

- Increase recording density
- Reduce bit volume $V$
- Reduce writing power
- Thermal stability: $\Delta E = KV$
- Writing: $H_{\text{writing}} \sim K$
- Increase $K$
- Reduce $K$

Research / Innovation

Storing: scalability of solid state magnetic recording

- Non volatility: $10^{-9}$ soft error rate in 10 years
- $\Delta E = KV \approx 60 k_B T$
- Today's best: FePt (L10) 2 nm
- Potential for non volatile « nano » spin electronics
- But $H_{\text{switching}} \sim 12$ Teslas!
- Field induced writing impossible
- Spin transfer writing requires high currents
- Precession speed $\sim 33$ GHz !!!!
1988: a major step into “Spin Electronics”

1988: The giant magnetoresistance (GMR) in magnetic multilayers

Fe/Cr multilayers

\[ R/R(H=0) \approx 80\% \]

A “bridge” between magnetic storage and electronics?

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The foundation of spin electronics

To directly "see" the "two-channel" conduction, one must make a material with internal structuration at the same scale as the \( \lambda \uparrow \) et \( \lambda \downarrow \) mean free path: the spin valve

F ferromagnetic layer
NM non magnetic layer (Cu, ..)
F ferromagnetic layer

"nano" input:
\[ \lambda \uparrow > \lambda \text{struct} > \lambda \downarrow \]
Giant magnetoresistance in multilayers

1988: Fert et al. (Orsay) and Grünberg et al. (Jülich)

- $\lambda_\parallel \ll \lambda_\perp \Rightarrow \rho_\parallel \gg \rho_\perp$
- parallel configuration $R_p < R_{AP}$
- antiparallel configuration

$\rho_\parallel = \rho_+\rho_-/(\rho_+ + \rho_-)$

Also: spin dependant "interface" scattering, reflection, ...

A first useful device: the "spin valve"

B. Dieny et al., PRB 1991

- "free" ferromagnetic layer (NiFe, CoFe,..)
- metallic (Cu) interlayer
- "pinned" ferromagnetic layer

$I$ in plane (CIP)

$R = R_0 - \Delta R/2 \cos(\theta)$

$\Delta R/R \parallel \sim 6 \text{ à } 20\%$

A convenient, compact, high sensitivity magnetic sensor!

... but ➔ low resistance, low signal amplitude ➔ planar geometry ➔ not well adapted to solid state electronics
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The tunnel junction

transmission by tunnel effect through a very thin (~1nm) barrier

electron spin is not affected by the tunneling
The magnetic tunnel junction

Ferromagnetic metal 1

Ferromagnetic metal 2

tunnel barrier (Al₂O₃, …)

Parallel state

Antiparallel state

spin dependant tunneling, \[ \text{MR} = \frac{(R_{AP} - R_P)}{R_P} \gg 1 \]

**Coherent tunneling through single crystal MgO tunnel junctions**


Fe(001)  
MgO(001)  
Fe(001)

![Image](image_url)

**giant $\Delta R/R$:**  
- 250% at 20K  
- 186% at 293 K

(also: Parkin et al., Nat. Mat 3 (2004))

**origin:** different attenuation for spin up and spin down electrons due to symmetry matching between metal and MgO states: up to 6000% predicted!  
[Butler et al, PRB63 (2001); Mathon et al., PRB 63 (2001); Butler & Gupta, Nat. Mat. 3, 845 (2004); Zhang et al., PRB 172407 (2004)]

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**The magnetic tunnel junction**  
M. Jullières, 1975  
J. Moodera, 1995

"free" ferromagnetic layer (NiFe, FeCo, FeCoB, …)  
tunnel barrier (ex: Al$_2$O$_3$, MgO) ~ 1 nm thick  
"pinned" ferromagnetic layer (NiFe, FeCo, FeCoB, …)

$\Delta R/R \uparrow\uparrow > 600 \% @ RT !!!$

(MgO single crystal tunnel barrier)

**practical value:**  
$\Delta R/R \sim 100-180 \%$  
for $RA \sim 3-50 \Omega \cdot \mu$m$^2$

A "vertical", high signal device for high density electronics!
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**The magnetic RAM (M-RAM)**

→ Magnetic Random Access Memory (M-RAM) (IBM, NVE, ... > 1996)

"0"

"1"

Principle:
- store binary information on arrays of magnetic tunnel junctions connected by conducting lines,
- that serve to address each cell individually for reading and writing
The magnetic RAM: practical implementation

"0"

+ "1"

practical MRAM cell:
"1T1MTJ" architecture for "reading"

incomplete integration of the writing function:
needs magnetic field created by independent line for writing

MRAM: writing / Stoner-Wohlfarth scheme

OR ...

Transistor ON
Magnetic RAM: "Savtchenko" toggle writing mode

- free layer = synthetic antiferromagnet
- current lines at 45 deg. of easy axis
  ➔ toggle switching mode


But: high currents (several mA) needed for writing !!!

- excellent immunity to program errors
  (cf Korenvski, APL 86 (2005))

- 4 Mbits Freescale demo:
  - 0.18 µm CMOS
  - ~47 F^2 cell size
  - 25 ns read/write cycle time
  - 3.3 V

(Andre et al., IEEE JSSC 40, 301 (2005))
Magnetic RAM: reducing $I_{\text{writing}}$

Sending a current in a conducting line is not a very efficient way of creating a magnetic field on a nano-element !!!!

- channeling the magnetic field using magnetic "cladding"

- gain of a factor of $\sim 2$ on the field/current ratio
- limits the stray field on half-addressed cells
- other "tricks" can help gain additional factors, up to ????

Freescale: 1rst MRAM product in 2006

Named "Product of the Year" [Electronics Products Magazine, Jan. 2007]

- in 2007: achieved army specifications ➔ automotive applications
- NEW in Nov. 2008: spin off company EVERSPIN
  - new products, target: battery backed SRAM
"Field induced magnetic switching":
downscaling prospect

Field induced switching:
• requires a current in a conducting line
• electromigration limit \(10^7\) A/cm\(^2\) \(\sim\) 100 mA/\(\mu\)m\(^2\)

@ constant \(j\): available \(H_{\text{write}}\) decreases \(\sim\) as \(F\)

 realistic estimation for 2 different width \(W\) of magnetic element:
\(W = 4/3 \times F\) and \(2 \times F\)

A “conventional” answer:
the thermally assisted writing in TAS-MRAM

From a “0” ..... ... to a “1”

Exchange biased storage layer is SAF/AF multilayer

Altis Semiconductors, Quimonda:
demo at IEDM Dec 2006 with 2 bits/cell
CMOS integration of TAS-MRAM

analytical model for 2ns pulse and 140K temperature rise

required writing power for bit dia. = (4/3)F
available power with Wt = (4/3)F
available power with Wt = 3 F

becomes more favorable when F decreases
condition much relaxed by using bipolar transistor (cf PC RAM)
issues remaining:
- match thermal stability with heat sensitivity in the cell
- still needed: a magnetic field from a conducting line

required switching current for MTJ width W_{MTJ} = 4/3 F

available current for 2 transistor widths:
W_t = 3 F
W_t = 4/3 F

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The Spin Transfer Torque mechanism

- L. Berger, PRB 54, 9353 (1996)

\[ \text{In the ferromagnetic layer: exchange interaction between e\textsuperscript{\textminus} spin and } M \]

\[ \text{\& the incoming electrons lose their transverse spin angular momentum to the magnetization } M \text{ of the ferromagnetic layer}\]

\[ \text{\& conservation of total angular momentum} \]

\[ \text{\& torque applied on } M \]

\[ \text{\& switching beyond a threshold } J_c \text{ in current density: scalable} \]

Writing: Spin Transfer Torque switching


Writing "0"

Writing "1"

Writing by a bipolar current density with \( J_c^+ \) and \( J_c^- \)
Magnetization switching by spin transfer in MgO tunnel junctions


![MgO tunnel junctions diagram]

Fig. 1. (a) Schematic drawing of the cross section of fabricated MTJ. The thickness of MgO is fixed as 6.85 nm. (b) Scanning electron microscopy image of a pillar after milling showing that the area of the fabricated pillar is 80 x 240 nm².

**ex. of good compromise:**

\[ \text{TMR} \sim 80\% \text{ for } T_{\text{anneal}} \sim 300^\circ\text{C} \]

\[ \langle J_c \rangle \sim 8 \times 10^5 \text{ A/cm}^2 \]

spin torque MRAM by SONY

SONY, IEDM Conference, Dec. 2005

A way towards very high density, fast MRAM, with potential for downscaling down to 20nm or less!

A true "solid state" integration of R/W and magnetic media!
From conventional MRAM... to "spin transfer" MRAM

- simple “integrated” architecture, above CMOS technology,
- “high” density (<16 F²), potential for downscaling down to 20nm
- “fast” (40-100 ns) M-RAM: main advantage of M-RAM versus other NVM RAM...

- can we reach high operation speed?
- will it be reliable?

Precession of the magnetization and spin transfer

The Landau-Lifshitz-Gilbert (LLG) equation

\[
\frac{dM}{dt} = -\gamma \mu_0 \left( \mathbf{M} \times \mathbf{H}_{\text{eff}} \right) + \alpha \left( \mathbf{M} \times \frac{d\mathbf{M}}{dt} \right)
\]

+ the "spin transfer torque"

\[
-G \cdot \mathbf{M} \times (\mathbf{M} \times \mathbf{p})
\]

≠ 0 only if \( M \) and \( p \) are non colinear

\( f_0 \approx 2.8 \text{ GHz} / \text{kOe} \)

Switching threshold \( J_c \): ~ when negative friction overcomes damping
Macrospin dynamics of spin transfer writing


\[ \text{thermal excitation spreads the initial orientation} \]

\[ + G j \dot{M} \times (\dot{M} \times \dot{p}) \]
\[ = 0 \text{ if } \dot{M} \text{ and } \dot{p} \text{ are colinear} \]

Devolder et al., PRB 75, 64402 (2007)

Switching by spin-transfer torque vs field

Spin-Transfer Torque
(friction-gradient driven switching)

Field
(Energy-gradient driven switching)
Routes towards fast spin transfer writing

Thermally assisted spin transfer switching:

- $J \approx J_c$
- $t_{\text{pulse}} \sim 10 \text{–} 100 \text{ ns}$ (cf demos)

Precessional spin transfer switching:

- $J > J_c$
- $t_{\text{pulse}} \leq 1 \text{ ns}$
- control thermal fluctuations
  - non zero initial torque

- Ito et al., APL89, 252509 (2006)
- etc...

STT MRAM main configurations

© Y. Suzuki

$\alpha = 0.1, k_2 = 0.0$
$\alpha = 0.1, k_2 = 0.15$
$\alpha = 0.1, k_2 = 0.42$
CMOS integration of spin–RAM: writing

compatibility with ITRS roadmap

<table>
<thead>
<tr>
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<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Node (F in nm)</td>
<td>90</td>
<td>65</td>
<td>45</td>
<td>32</td>
<td>22</td>
</tr>
<tr>
<td>Nominal voltage (V_n)</td>
<td>0.9</td>
<td>0.8</td>
<td>0.7</td>
<td>0.6</td>
<td>0.5</td>
</tr>
<tr>
<td>Max current (µA) at 25°C for transistor width Wt=F</td>
<td>47.7</td>
<td>37.05</td>
<td>34.65</td>
<td>24.96</td>
<td>20.24</td>
</tr>
<tr>
<td>R_n = V_n/I_d,sat for Wt=F (kΩ)</td>
<td>18.9</td>
<td>21.6</td>
<td>20.2</td>
<td>24.0</td>
<td>24.7</td>
</tr>
</tbody>
</table>

bipolar use of the NMOS transistor

CMOS integration of STT MRAM

requires a “bipolar” use of the NMOS transistor

large variation of resistance during the write process (Sony)

within ITRS 2003 roadmap
CMOS integration of STT MRAM

\[
J_{SW(a)} \approx J_{ON} = \left( \frac{2e}{h} \right) \alpha t_p M_s \left( \frac{\mu_0 M_s}{2} + \mu_H H_m \right)
\]

approximate switching current density for in plane magnetization

\[ \eta \]
in plane shape anisotropy

\[ \eta \]
thermal stability factor

\[ \eta \]
current density should not depend much on size !!!!

Scalability of Spin-RAM: writing

\[ \text{transistor width: } (4/3) F \text{ for high density memory} \]

magnetic element:

\[ (4/3) F \text{ (min)} \]

writing speed:

\[ \sim 20-40 \text{ ns} \]

tunnel junction:

\[ R_{\uparrow \uparrow} \sim \frac{R_{\text{transistor}}}{2} \]

RA \sim 1-20 \Omega \mu m^2, within reach

\[ \text{also good for reading} \]

transistor's limit

\[ \text{I}_{WR} \text{ (SONY, IEDM 2005)} \]

\[ \text{I}_{WR} \text{ (lab's best, 2006)} \]
CMOS integration of STT MRAM

Available current for 2 transistor widths:
- \( W_T = 3 \, \text{F} \)
- \( W_T = 4/3 \, \text{F} \)

More favorable than in plane case, if similar values of \( \alpha/\eta \) are obtained

Perpendicular STT RAM

Toshiba Develops MRAM Device, Opening Way to Gb Capacity
Nikkei Electronics Asia, November 7, 2007

With TMR \( \sim 100\% \) and \( j_C \sim 3 \times 10^6 \, \text{A/cm}^2 \)
**Summary: Spin - RAM specifications**

<table>
<thead>
<tr>
<th></th>
<th>Products / Demos</th>
<th>Predicted</th>
<th>Position vs CMOS</th>
</tr>
</thead>
<tbody>
<tr>
<td>Cell size</td>
<td>25 – 80 F²</td>
<td>&lt; 16 F²</td>
<td>&gt;&gt; NAND</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>&lt;&lt; SRAM</td>
</tr>
<tr>
<td>Technology</td>
<td>Above CMOS</td>
<td></td>
<td>embedded RAM</td>
</tr>
<tr>
<td>Speed</td>
<td>~ 40 ns (2.7 ns)</td>
<td>~ ns</td>
<td>~SRAM</td>
</tr>
<tr>
<td>Endurance</td>
<td>10¹⁵</td>
<td>~ infinite</td>
<td>&gt;&gt; NAND</td>
</tr>
<tr>
<td>Non volatility</td>
<td>&gt; 10 years</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Scalability</td>
<td>130 nm</td>
<td>20 nm</td>
<td>?</td>
</tr>
</tbody>
</table>

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CMOS Logic Circuits

- Low power (near zero static power)
- High density (45nm, 2007)
- High Speed (>Some GHz)
- ...

ASIC

Application-Specific Integrated Circuit

- High mask cost (1.4M$/Mask @ 90nm)
- Long delay to correct a bug
- Long time to market

LEAKAGE CURRENTS

Programmable logic devices

ASIC

Programmable Logic

LUT: Look Up Table

a b s
0 0 0
0 1 0
1 0 0
1 1 1

a = Adr 0
b = Adr 1

config.: EEPROM, Flash

SRAM
Low standby Power
Programmable logic devices

Non volatile, multi-core logic:
- are powered only the core that need to operate
- others preserve state and start « instantly » when powered on

100% 61% 14% 0%

Towards a magnetic FPGA

“switches” and “logic blocs” (CLB) are made:
- non volatile
- programmable
by Spin- MRAM elements

FPGA Logic Circuits

Configuration

SRAM

Static RAM based FPGA
- High computing speed
- Infinite programming endurance

CMOS intrinsic memorizing constraint: Data Volatility
- Long latency at each start or restart
- High standby power (>30% for 90nm)
- Data loss in case of power failure
- Uneasy dynamical reconfiguration
replace Flash and SRAM by a non volatile memory (NVM) directly embedded inside the look up table

replace the standard Flip-Flop by a non volatile one
### Spin-RAM based Non-volatile Flip Flop

- **Master slave flip-flop based on spin transfer switching**
- **Non volatile**
- **Instant on/off**
- **Record all intermediate calc. steps**

**If:**
- CMOS compatible $I_{\text{wr}}$
- Writing speed at processor's rate (~3 GHz)

**→** e-MRAM could enter the CPU!!!

**Sense Amplifier**


- **~ non volatile SRAM**
- **Fast reading possible**
- **Writing ?**

**Electrical simulation**

- **MTJ model (V. Javerliac et al., MMM, 2006)**
- **STMicroelectronics 90nm design kit**

- **$W_p=0.12\mu m$**
- **$W_n=0.12\mu m$**
- **TMR=80%**
- **$R(0)=8.9\Omega$**

**Sense**

- **Out**
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Another promising scientific breakthrough:
current induced domain wall motion

- Thick wall
  - Electrons
  - Domain wall (DW) motion
  - Transfer of spin angular momentum
  - (Grollier, APL 2004, Vernier, EuroPhys. 2005, Thiaville, cond-mat 407628, ...)

- Thin wall
  - Electrons
  - DW motion
  - Transfer of momentum
  - Berger (’84,’92), Tatara & Kohno (2004)

Current induced domain wall propagation: downscaling prospect

- Energy barrier \( KV > k_B T \) if \( V \propto F^2 \), then \( K \propto 1/F^2 \)

- Writing current:
  - \( w = F = 90 \text{ nm}, t = 10 \text{ nm}, j_c = 10^6 \text{ A/cm}^2 \Rightarrow I_{WR} \sim 9 \text{ µA} \)
  - (standard transistor @ \( F = 90 \text{ nm} \): \( I_{MAX} \sim 0.5 \text{ mA/µm} \))
  - (?) Scaling of the writing current density vs non volatile DW trapping
One proposition of "Solid State Hard Disk"

Shiftable magnetic shift register and method of using the same
S.S.P. Parkin
US patent 6,834,005B1
of Dec. 21, 2004

same data organization as in HD,
but no moving part

- fast access time!
- domain wall speed: up to ~100m/s
- high data rates!

A new approach to magnetic storage

Shiftable magnetic shift register and method of using the same
S.S.P. Parkin - US patent 6,834,005B1 pub. Dec. 21, 2004
Submicrometer Ferromagnetic NOT Gate and Shift Register,
Multiple layer magnetic logic memory device

- Information is stored in a magnetic strip, as contiguous magnetization domains.
- Domains are made to migrate synchronously from programming head to reading head with either an external magnetic field or a current injected in the strip (spin transfer effect).
Russel Cowburn et al.


storage ring (shift register with one input)

<table>
<thead>
<tr>
<th></th>
<th>DW logic</th>
<th>Flash</th>
</tr>
</thead>
<tbody>
<tr>
<td>Effective area cell size</td>
<td>1 – 2 $\mu$m$^2$</td>
<td>5 – 10 $\mu$m$^2$</td>
</tr>
<tr>
<td>Cell write time</td>
<td>5 – 10 ns</td>
<td>~100 ns</td>
</tr>
<tr>
<td>Write endurance</td>
<td>Unlimited</td>
<td>10,000 cycles</td>
</tr>
</tbody>
</table>

3D storage

Silicon CMOS containing field generation, field sensing, multiplexing etc

Spin electronics today:

a giant move towards integration …

Longitudinal Hard Disk recording
With spin valve head (1997)

Spin-RAM, SONY, IEEE 2005
... in a short span of time

1988: GMR discovered
1991: "spin valve"
1995: "practical TMR"
1997: product, SV HD read head (IBM)
1996-2000: "spin transfer" predicted/observed
1998-2000: "spin transfer" predicted/observed
2005: product, TMR HD read head (Sagami)
2005: product, TMR HD read head (Fujitsu)
2006: product, MRAM (Freescale)
2010: spin-TMR product?? (RENESA, NEC, SONY, Samsung, CROCUS)

1990 2000 2010
10 years
10 years

Perspective: a new paradigm for “spintronics”
electron: charge + spin + phase coherence

spin dependent transport in multilayers controlling magnetization by “currents” (w or w/o charges)

• spin dependent quantum transport
• coherence and Quantum Information?

mesoscopic spintronics from uniformly magnetized nanostructures to non collinear magnetization structures (vortex, domain walls, …)

a wide field for research!

materials, hybrid stacks, nanotechnologies, devices, nano-architectures, device integration