A stacked SONOS technology with crystalline gate-all-around Si nanowires for full 3D integration

T. Ernst, A. Hubert, G. Molas, B. de Salvo

CEA-LETI, MINATEC, Grenoble, France

thomas.ernst@cea.fr
Outline

- **Introduction**
- Stacked GAA SONOS crystalline nanowire memory
- Comparison of the 3D architectures
- Towards a new full 3D memory structure
- Conclusion
Main issues to scale NAND memories below the 30nm (32Gbit):

- Photolithography (EUV) availability
- Intrinsic physical, electrical and reliability limits
- Difficulty to maintain the current pace of cost reduction
“Traditional” 3D Memory Architecture (1/2)

3D Stacked NAND

Main limit → Increasing the number of stacked layers, Bit cost reduction limited by yield loss and area penalty

[SAMSUNG IEDM06]
“Alternative” 3D Memory Architectures (2/2)

P-BiCS
*Toshiba*  
[Katsumata VLSI 09]

TCAT
*Flash*
*Samsung*  
[Jang VLSI 09]

VG-NAND,  
*Samsung*  
[Kim, VLSI 09]

Main limit → All based on polycrystalline channels, thus limiting NAND performance
Our Approach

Epitaxial (Si/SiGe) superlattice & selective SiGe etching

⇒ Gate-All-Around (GAA) SONOS memory with « crystalline » Si nanowire channels (down to 6nm diameter)
⇒ Comparison with SONOS FinFET cells (FinFlash)
⇒ Towards a full 3D memory with crystalline SiNW channels & straightforward 3D addressing strategy (BL, AG, WL)

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Process flow of the stacked GAA SONOS crystalline nanowires memory

1. Selective epitaxy of (Si/SiGe)

2. Si anisotropic dry etching
   + SiGe dry isotropic etching

2.1. Dry sacrificial oxidation
   + H2 annealing

3. ONO deposition
   O/N/O = 6/5/8nm

4. Poly-Si N+ deposition
   + Chemical Mechanical Polishing
   + Gate etching
   + S/D implantation
   + Nitride spacers
   + S/D salicidation
   + BEOL

A. Hubert et al. IEDM 2009
Transfer Characteristics of GAA SONOS SiNW

Good Short Channel Effect control

\( I_{\text{ON}}/I_{\text{OFF}} \) ratio \( \sim 10^8 \)

\( d_{\text{Si}} \sim 6\text{nm} \)
\( L_{\text{G}} \sim 80\text{nm} \)

17nm EOT

\( V_D = 1\text{V} \)
\( V_D = 0.05\text{V} \)

\( I_{\text{ON}} = 5.0\mu\text{A} \)
\( I_{\text{OFF}} = 84\text{fA} \)

SS = 70mV/dec
DIBL = 41mV/V
Program/Erase of GAA SONOS SiNW

Very large programming window
FN achievable thanks to NW geometry (O/N/O = 6/5/8nm)

A. Hubert et al. IEDM 2009
Programming window of GAA SONOS SiNW

\[ \Delta V_{Th} = 7.4V \ (10\mu s/100\text{ms programming times}) \]
Suitable for multi-level applications

A. Hubert et al. IEDM 2009
Endurance GAA SONOS SiNW

$\Delta V_{th} = 5V$ after $10^4$ cycles (with 0.8V $V_{th}$ shift)

Program: 14V, 10$\mu$s
Erase: -16V, 10ms

A. Hubert et al. IEDM 2009
Room Temperature data-retention of GAA SONOS SiNW

No degradation of the retention after 10K cycles

A. Hubert et al. IEDM 2009
High Temperature data-retention of GAA SONOS SiNW

18% charge loss @ 25°C, 50% charge loss @ 200°C

A. Hubert et al. IEDM 2009
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Comparison of GAA SONOS SiNW and FinFLASH

Same gate stack (O/N/O = 6/5/8nm) and Si-fin height

A. Hubert et al. IEDM 2009
Channel characteristics of the 3 structures

GAA SONOS NW → Improved $I_{OFF}$, SS, DIBL
Higher $I_{ON}$ with FinFlash and 4Wires
Programming windows

GAA SONOS Nanowire with small cylinder shape greatly enhances the programming efficiency

A. Hubert et al. IEDM 2009
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**Φ-Flash: concept**

**Stacked Nanowires**

*Excellent electrostatic control*

*High $I_{\text{ON}}$ current*

+ Limitation of gate isotroping etching

+ Possible use of independent gates

A. Hubert et al. IEDM 2009
Φ-Flash: process flow

1. Selective epitaxy of (Si/SiGe)
2. Si anisotropic dry etching
   + SiGe dry isotropic etching
3. ONO deposition = 6/5/8nm
4. Poly Si N+ deposition
   + Chemical Mechanical Polishing
   + Gate etching
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4-Stacked 3D SONOS NW
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New 3D memory architecture with crystalline channels

Technology can be derived from the stacked GAA SONOS Silicon nanowire developed process
Full 3D memory: current process developments

Successful separation of the channels along the 10µm nanowires without sticking

Very high density can be achieved by epitaxy
Summary

- First time Stacked GAA SONOS crystalline Si nanowires memory integrated (up to 4 levels) with 6nm diameter shows:
  - excellent programming window up to 7.4V (@$V_P = 18V$ for 10µs)
  - excellent retention
  - $I_{ON}/I_{OFF} \sim 10^8$

- Enhanced memory performances for GAA SONOS nanowires device compared to FinFlash

- Towards a full 3D memory with crystalline Si channels:
  - selective oxidation of SiGe compared to Si
  - large number of epitaxial (Si/SiGe) superlattice
Acknowledgements

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